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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,203	03/17/2004	Roy J. Blazek	34282	3763

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EXAMINER

GREEN, PHILLIP

ART UNIT	PAPER NUMBER
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2823

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/802,203

Applicant(s)

BLAZEK ET AL.

Examiner

Brook Kebede

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 May 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Rutt (US/3,772,748).

Re claim 1, Rutt discloses a method of creating a monolithic circuit structure (see Fig. 1 and Col. 2, lines 11-55), the method comprising the steps of: printing a circuit component onto an individual layer of substrate (see Fig. 1-6); firing the individual layer of substrate and the circuit component printed thereon; adjusting the circuit component as necessary to achieve a desired degree of precision; applying a bonding agent to the individual layer of substrate and assembling the individual layer of substrate with one or more other layers of substrate; and firing the assembled individual layer of substrate and one or more other layers of substrate together to activate the bonding agent, thereby bonding the individual layer of substrate to the one or more other layers of substrate and creating the monolithic circuit structure (see Figs. 1-6 and related text in Col. 2, line 11 – Col. 14, line 29).

Re claim 2, as applied to claim 1, Rutt discloses all the claimed limitations including wherein the circuit component is selected from the group consisting of: resistors, **capacitors**, and inductors (see Figs. 1-6 and related text in Col. 2, line 11 – Col. 14, line 29).

Re claim 3, as applied to claim 1, Rutt discloses all the claimed limitations including wherein the circuit component is placed printed onto the individual layer of substrate by screen-printing (see Figs. 1-6 and related text in Col. 2, line 11 – Col. 14, line 29).

Re claim 4, as applied to claim 1, Rutt discloses all the claimed limitations including wherein the individual layer of substrate and the one or more other layers of substrate are pre-fired thick film ceramic substrate (see Figs. 1-6 and related text in Col. 2, line 11 – Col. 14, line 29).

Re claim 5, as applied to claim 4, Rutt discloses all the claimed limitations including wherein the individual layer of substrate and the one or more other layers of substrate are standard alumina thick film ceramic substrates (see Figs. 1-6 and related text in Col. 2, line 11 – Col. 14, line 29).

Re claim 6, as applied to claim 1, Rutt discloses all the claimed limitations including wherein the bonding agent is a thick film glass (see Figs. 1-6 and related text in Col. 2, line 11 – Col. 14, line 29).

Re claim 7, Rutt discloses a method of creating a multi-layered monolithic circuit structure, the method comprising the steps of: printing a circuit component onto an individual layer of thick film ceramic substrate; firing the individual layer of thick film ceramic substrate and the circuit component printed thereon; trimming the circuit component as necessary to achieve a desired degree of precision; applying a bonding agent to the individual layer of thick film ceramic substrate and assembling the individual layer of thick film ceramic substrate with one or more other layers of thick film ceramic substrate; and firing the assembled individual layer of thick film ceramic substrate and one or more other layers of thick film ceramic substrate

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together to activate the bonding agent, thereby bonding the individual layer of thick film ceramic substrate to the one or more other layers of thick film ceramic substrate and creating the multi-layered monolithic circuit structure (see Figs. 1-6 and related text in Col. 2, line 11 – Col. 14, line 29).

Re claim 8, as applied to claim 7, Rutt discloses all the claimed limitations including wherein the plurality of circuit components are selected from the group consisting of: resistors, capacitors, and inductors.

Re claim 9, as applied to claim 7, Rutt discloses all the claimed limitations including wherein the individual layers of thick film ceramic substrate are standard alumina thick film ceramic substrate (see Figs. 1-6 and related text in Col. 2, line 11 – Col. 14, line 29).

Re claim 10, as applied to claim 7, Rutt discloses all the claimed limitations including wherein the bonding agent is a thick film glass (see Figs. 1-6 and related text in Col. 2, line 11 – Col. 14, line 29).

Re claim 11, Rutt discloses a method of creating a multi-layered monolithic circuit structure, the method comprising the steps of: screen-printing a plurality of circuit components onto a plurality of individual layers of thick film ceramic substrate; firing the individual layers of thick film ceramic substrate and the circuit components screen-printed thereon; trimming the circuit components as necessary to achieve a desired degree of precision; applying a thick film glass bonding agent to the individual layers of thick film ceramic substrate and assembling the individual layers of thick film ceramic substrate; and firing the assembled individual layers of thick film ceramic substrate to sinter the thick film glass bonding agent, thereby bonding the

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individual layers of thick film ceramic substrate together and creating the multi-layered monolithic circuit structure (see Figs. 1-6 and related text in Col. 2, line 11 – Col. 14, line 29).

Re claim 12, as applied to claim 11, Rutt discloses all the claimed limitations including wherein the plurality of circuit components are selected from the group consisting of: resistors, capacitors, and inductors (see Figs. 1-6 and related text in Col. 2, line 11 – Col. 14, line 29).

Re claim 13, as applied to claim 11, Rutt discloses all the claimed limitations including wherein the individual layers of thick film ceramic substrate are standard alumina thick film ceramic substrate (see Figs. 1-6 and related text in Col. 2, line 11 – Col. 14, line 29).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rutt (US/3,772,748) in view of Naumov et al. (US/6,875, 950).

Re claim 14, Rutt discloses a method of creating a multi-layered monolithic circuit structure, the method comprising the steps of: screen-printing a plurality of circuit components onto a plurality of individual layers of substrate, wherein the circuit components are selected

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from the group consisting of: resistors, capacitors, and inductors, and wherein the individual layers of substrate are standard alumina thick film ceramic substrate; firing the individual layers of substrate and the circuit components screen-printed thereon; trimming the circuit components as necessary to achieve a desired degree of precision; applying a thick film glass bonding agent to the individual layers of substrate and assembling the individual layers of substrate; and firing the assembled individual layers of substrate to sinter the thick film glass bonding agent, thereby bonding the individual layers of substrate together and creating the multi-layered monolithic circuit structure (see Figs. 1-6 and related text in Col. 2, line 11 – Col. 14, line 29).

However, Rutt does not explicitly disclose trimming the circuit component as necessary to achieve a desired degree of precision

Naumov discloses the laser trimming of passive circuit elements such as resistors, capacitors and inductors. (Note: Abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicants') claimed invention was made to use the laser trimming taught by Naumov in the invention of Rutt in order to achieve narrow final resistor tolerances. (Note: Naumov, Col. 10, line 5-9).

### ***Response to Arguments***

5. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

6. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

***Correspondence***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*Brook Kebede*

Brook Kebede  
Primary Examiner  
Art Unit 2823

BK  
July 22, 2006